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APPLICATION

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TITLE: IMPRINT SUPPRESSION CIRCUIT SCHEME

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Imprint Suppression Circuit Scheme

Field of the Invention

The present invention relates to imprint suppression in ferroelectric capacitors.

Background of the Invention

A ferroelectric random access memory (FeRAM) uses a ferroelectric capacitor to store memory cell data. Each memory cell stores a logic state based on electric polarization of the ferroelectric capacitor. The ferroelectric capacitor has a dielectric including a ferroelectric such as PZT (lead zirconate titanate) between two electrodes. When a voltage is applied to each plate of the ferroelectric capacitor, the ferroelectric is polarized in a field direction. A voltage above the coercive voltage changes the polarization state of the ferroelectric capacitor. The ferroelectric capacitor operates with hysteresis, and current flows to the capacitor in accordance with the polarization state. If the applied voltage is greater than the coercive voltage, the ferroelectric capacitor will change the polarization state in accordance with a polarity of the applied voltage. The polarization state can be maintained after removing the power source, resulting in non-volatility. The ferroelectric capacitor changes between the polarization states within a short time, e.g., about 1 ns. The programming time of the ferroelectric memory device is faster than that of most other non-volatile memory devices such as erasable programmable read only memories (EPROMs), electrically erasable programmable read only memories (EEPROMs), and flash EEPROMs.

The performance of an FeRAM degrades due to aging of the ferroelectric capacitor. One major aging mechanism in such ferroelectric capacitors is imprint. Imprint is the enhancement of one stored polarization state and the weakening of the reversed state. In the worst case, due to aging, an imprinted ferroelectric capacitor cannot be reversed, causing the memory cell to fail. Two types of imprint causing the aging effect are static imprint, which is caused by the storage of certain data over an extended period of time, and dynamic

imprint, which is caused by the continuous reading and writing back of the same data. It would be desirable to provide a circuit scheme for reducing the effect of both of these imprint aging mechanisms.

Summary of the Invention

The present invention provides a circuit scheme for reducing the effect of both the static and dynamic imprint aging mechanisms. The physical data in a memory cell, and thus the polarization state of the ferroelectric capacitor, is reversed each time the cell is read, thus reducing the imprint effect drastically in typical applications and significantly increasing the reliability of the memory cells.

A ferroelectric memory array includes a plurality of memory pages each formed of a plurality of ferroelectric memory cells. The ferroelectric memory cells are supplied by common word lines. Status memory cells are connected to each of the plurality of memory pages, each status memory cell stores the status of the memory page to which it is connected. A plurality of sense amplifiers each receives inputs from a pair of bit lines. Each of the bit lines receives inputs from the ferroelectric memory cells of a plurality of the memory pages. The sense amplifiers write back data into the memory cells and status cells in reversed states following read operations.

Brief Description of the Figures

Further preferred features of the invention will now be described for the sake of example only with reference to the following figures, in which:

FIGURE 1 shows a part of a ferroelectric memory (FeRAM) array comprising a plurality of ferroelectric memory cells at cross points of word lines and bit lines.

FIGURE 2 shows a sense amplifier circuit of the present invention.

FIGURES 3 and 4 show the regeneration of logical data from the physically stored data.

Detailed Description of the Embodiments

The present inv_ntion reduces the ffect of both the static and dynamic imprint aging mechanisms by frequently reversing the stored data and thus frequently reversing the internal polarization of the ferroelectric material.

FIGURE 1 shows a part of a ferroelectric memory (FeRAM) array 101 comprising a plurality of ferroelectric memory cells 103 at cross points of word lines (WL) 107 and bit lines (BL) 105. The bit lines 105 are connected as pairs, for example a pair 108 consisting of the bit line 105 and a bit line 106, to differential sense amplifiers 109. For reading and writing a plate line is used (not shown). FeRAM architectures other than the particular one shown in FIGURE 1 can also be used with the present invention.

In the array 101 of FIGURE 1, the plurality of cells 103 are connected to each word line 107. Each of these plurality of cells 103 forms a "memory page" 113 and is used to store the data. According to the present invention, an additional memory page status cell 111 is connected to each of the pages and is used to store the status of the page to which it is connected. The status of each memory page 113 stored by each of the memory page status cells 111 can be "true" (D) or complement (/D). The page status cells 111 are connected together forming a pair of IPSBLs (imprint status bit lines) 110, 112. The pair of IPSBL's 110, 112 provides outputs to an imprint status circuit 115. The imprint status circuit 115 is comprised of imprint sense amplifiers (IPSA), as illustrated in FIGURE 3, and provides a control signal 114 to the differential sense amplifiers 109.

Memory cells 103 forming the same bit line (e.g. the bit line 105) are part of memory pages (e.g. the memory page 113) having page status cells (e.g. the page status cell 111) forming a common IPSBL (e.g the IPSBL 112). Thus, memory cells 103 of the bitline 105 supplying outputs to one of the differential inputs of the sense amplifier 109 will belong to memory pages having memory page status cells supplying outputs to a common imprint status circuit 115 input.

After each read operation of the memory pages 113, the data is written back both into the memory cells 103 and the memory page status cells 111 in the data's reversed state. This reversed write-back is done by the inventive

sense amplifier circuit 109 of FIGURE 1 which is shown in more detail in FIGURE 2. FIGURE 2 includes two inverters 211, 213 activated by a sense amplifier enable signal (SAEN) 215. Other similar amplifier circuits can also be used.

During a read operation a signal RD/WR 203 is at high potential. This results in the bit line BL<n+1> 106 being connected to a node of the sense amplifier (node SA) 207. It also results in the bit line BL<n> 105 being connected to a node of the sense amplifier (node /SA) 209. Thus, the bit lines 105, 106 are directly connected to the sense amplifier 109.

During write back, the signal RD/WR 203 is at low potential. This results in the bit line BL <n+1> 106 being connected to the node /SA 209. It also results in the bit line BL<n> 105 being connected to the node SA 207. Thus, the bit line pair 108 is intersected. This scheme reverses the physical data in the storage cells 103 during each read access.

Although the physical data is reversed, the logical data which is read from the entire memory array 101 must stay the same. This is accomplished by inserting XOR gates 205 in the data path.

FIGURES 3 and 4 show the regeneration of the logical data 309 from the physically stored data 305 stored in the memory cells 103. The sense amplifier SA 307 represents the portion of the differential sense amplifier 109 to the left of the dashed line. If the physical data is true data (D), as in FIGURE 3, the memory page status cells 111 store logical "0" and the read data passes the XOR gate 205 directly. If the physical data is complement data (/D), as in FIGURE 4, the memory page status cells 111 stores a logical "1" and the read data is reversed by the XOR gate 205.

In both cases the data on the main data bus (DQ) 303 reflects the original logical data (D) 305 which was stored in the memory cell 103.

In a write operation, the data 305 is written directly into the memory cell 103 (true data, D) and the status cell 111 is set to "0", reflecting this status.

Although the invention has been described above using particular embodiments, many variations are possible within the scope of the claims, as will be clear to a skilled reader.